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10/618,284	07/11/2003	Peter Brookes	15114H-067600US	4798

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,284	BROOKES ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-16 and 18-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-16, 18-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-16, 18-33 have been presented for examination.

Claims 2 and 17 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 8 August 2006 have been fully considered but they are not persuasive.

i) Applicant argues that the reference does not disclose "simulating only certain hardware components using a software model." This limitation is not present in the claim. The Applicant appears to be referring to the limitation "simulating the software element and the second hardware component in a second simulation using a software model." However, the reference discloses in Column 30, Lines 47-61, for example, **"For a variety of reasons including performance and simulation monitoring, the user can force certain components that would otherwise be modeled in hardware to stay in software."**

ii) Applicant argues that the reference does not disclose "running a first and second simulation asynchronously with the second simulation running ahead of the first simulation." However the reference discloses in, for example, Figure 17 and its corresponding description both asynchronous simulation as well as asynchronous data input.

iii) Applicant argues that the reference does not disclose "allowing for more rapid simulation of software instructions in a software model for an embedded hardware component in a hardware environment." In response to applicant's argument that the reference does not disclose this limitation, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. The term "allowing" renders the limitations following the term as intended use and is therefore not

given patentable weight. It is noted that the reference is also designed to provide more rapid simulation of a system, see Column 8, Lines 1-13 for example.

iv) Applicant argues that the reference does not disclose "the software debugger having no knowledge of the connection between the first and second simulations." First the phrase "having no knowledge" renders the claim vague and indefinite, see 112 2nd rejection below. Second, it is unclear how this limitation creates a patentable distinction with the prior art since the prior art discloses inter-process communications, see Column 87, Lines 50-64, for example.

v) Applicant argues that the reference does not disclose "an input/output device model in contact with a terminal emulator running an interactive program, whereby information can be transferred to the input/output device model and subsequently obtained by a software model through a polling procedure." However the reference discloses in Column 22, Line 29-42 as well as in the Abstract **"The RCC computing system also contains clock logic (for clock edge detection and software clock generation), test bench processes for testing the user design, and device models for any I/O device that the user decides to model in software instead of using an actual physical I/O device. The user may decide to use actual I/O devices as well as modeled I/O devices in one debug session."** These sections indicate input/output device models with user control.

vi) Since no additional arguments were made regarding the 103 rejections of claims 13 and 27 the rejections are maintained.

vii) Please note, following Applicants amendment, the 101 and 112 2nd rejections provided below.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02. A process that consists solely of the manipulation of an abstract idea is not concrete or tangibles. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed.Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

3. **Claims 1, 3-16, 18-33 are rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1, 15, and 29 disclose hardware components as well as I/O devices. It is unclear if these components and devices are software representations of actual hardware or actual hardware. The broadest reasonable interpretation of the claims would result in the possibility that these components and devices are merely software and as such the claims would not produce a useful, concrete, and tangible result.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 15-28 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 contains the phrase ""having no knowledge" which renders the claim vague and indefinite.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-12, 14-26, 28-33 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **Lin et al. "Coverification System and Method", U.S. Patent No. 6,389,379,** hereafter referred to as **Lin.**

Regarding Claim 1:

Lin discloses A method for simulating a system which comprises a software element, and first and second hardware components, the software element being for execution on the second hardware component, and the first and second hardware components being operable to interact with one another, the method comprising the steps of:

simulating operation of the first hardware component in a first simulation in a hardware environment; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

and simulating the software element and the second hardware component in a second simulation using a software model; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

wherein the first simulation and the second simulation are implemented in separate processing threads and. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

wherein the first and second simulation run asynchronously, the second simulation running ahead of the first simulation allowing for more rapid simulation of software instructions in the software model. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57. Column 30, Lines 47-61)**

Regarding Claim 3:

Lin discloses A method as claimed in claim 1, wherein the first simulation and the second simulation are synchronised with a reference clock. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 4:

Lin discloses A method as claimed in claim 1, wherein the first and second simulations run in different respective simulation environments. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 5:

Lin discloses A method as claimed in claim 1, further comprising:

performing operations in the first simulation to set up an inter-process communications protocol connection therein; **(Column 87, Lines 50-64)**

connecting the second simulation to the interprocess communications protocol connection in the first simulation; **(Column 87, Lines 50-64)**

connecting a software debugger to the second simulation; **(Abstract. Column 1, Lines 33-49)**

and controlling the first simulation from the software debugger via the second simulation using the interprocess communications protocol. **(Abstract. Column 1, Lines 33-49)**

Regarding Claim 6:

Lin discloses A method as claimed in claim 1, further comprising:

performing operations in the first simulation to set up an inter-process communications protocol connection therein; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

connecting a software debugger to the communications protocol connection; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

and controlling the first simulation from the software debugger using the inter-process communications protocol. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 7:

Lin discloses A method as claimed in claim 5 or 6, wherein the inter-process communications protocol is TCP/IP and the connection is a TCP/IP socket. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 8:

Lin discloses A method as claimed claim 1, wherein the second hardware component includes a processor. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 9:

Lin discloses A method as claimed in claim 8, wherein the processor is an embedded processor. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 10:

Lin discloses A method as claimed in claim 1, wherein the hardware component includes processor peripheral devices. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 11:

Lin discloses A method as claimed in claim 10, wherein the peripheral devices are embedded. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 12:

Lin discloses A method as claimed in claim 1, wherein the first simulation is implemented using a hardware description language (HDL) simulation environment. **(Figure 26)**

Regarding Claim 14:

Lin discloses A method as claimed in claim 1, wherein the first hardware component is a programmable logic device. **(Column 63, Lines 4-10)**

Regarding Claim 15:

Lin discloses A method for controlling a simulation of a system using a software debugger, wherein the system comprises a software element, and first and second hardware components;

the software element being for execution on the second hardware component and the first and second hardware components being operable to interact with one another, the method comprising the steps of:

simulating the first hardware component in a first simulation; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

simulating the software element and the second hardware component in a second simulation; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

performing operations to set up an inter-process communications protocol connection; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

connecting the software debugger to the software model of the second simulation; and **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

controlling the first simulation from the software debugger through the software model of the second simulation using the inter-process communications protocol, the software debugger having no knowledge of the connection between the first and second simulations. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 16:

Lin discloses A method as claimed in claim 15, further comprising the step of:

connecting the software debugger to inter-process communications protocol connection. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 18:

Lin discloses A method as claimed in claim 15, wherein the inter-process communications protocol is TCP/IP and the connection is a TCP/IP socket. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 19:

Lin discloses A method as claimed in claim 15, wherein the step of simulating the second hardware component comprises simulating a processor and one or more peripheral devices with which the

one or more processors interact directly. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 20:

Lin discloses A method as claimed in claim 15, wherein the first simulation and the second simulation are implemented in separate processing threads. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 21:

Lin discloses A method as claimed in claim 15, wherein the first simulation and the second simulation run asynchronously. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 22:

Lin discloses A method as claimed in claim 15, wherein the first simulation and the second simulation are synchronised with a reference clock. **(Figures 1, 2, 3, 5, and 19)**

Regarding Claim 23:

Lin discloses A method as claimed in claim 15 wherein the first and second simulations are implemented in respective different simulation environments. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 24:

Lin discloses A method as claimed in claim 15, wherein the second hardware component includes embedded processors. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 25:

Lin discloses A method as claimed in claim 15, wherein the second hardware component includes embedded peripheral devices. **(Column 11, Line 59 – Column 12 Line 2)**

Regarding Claim 26:

Lin discloses A method as claimed in claim 15, wherein the first simulation is implemented using a hardware description language (HDL) simulation environment. **(Figure 26)**

Regarding Claim 28:

Lin discloses A method as claimed in claim 15, wherein the first hardware component is a programmable logic device. **(Column 63, Lines 4-10)**

Regarding Claim 29:

Lin discloses A method for providing an I/O interface for a simulation model to allow the simulation of interactive programs, the method comprising:

simulating a software element using a software model in a first processing thread; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

simulating an embedded input/output device within the simulation model to produce an input/output device model; **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

connecting the input/output device model to a terminal emulator using an inter-process communications protocol; **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

running an interactive program in the terminal emulator to transfer information to the input/output device model, and. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64. Figures 1, 2, 3, 5, and 19)**

polling the input/output device model for the transferred information using the software model. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57. Column 22, Lines 29-42.)**

Regarding Claim 30:

Lin discloses A method as claimed in claim 29, the method further comprising: providing separate processing threads for the embedded input/output device to allow concurrent user inputs and outputs. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 31:

Lin discloses A method as claimed in claim 29, wherein the inter-process communications protocol is TCP/IP. **(Abstract. Column 1, Lines 33-49. Column 87, Lines 50-64)**

Regarding Claim 32:

Lin discloses A method as claimed in claim 29, wherein the input/output device is a UART device. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Regarding Claim 33:

Lin discloses A method as claimed in claim 29, wherein the input/output device is an Ethernet MAC device. **(Figures 1, 2, 3, 5, and 19. Column 27, Lines 45- Column 28, Lines 57)**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claim(s) 13 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin in view of Kim et al. "An Integrated Hardware-Software Cosimulation Environment with Automated Interface Generation"**, hereafter referred to as **Kim.**

Regarding Claim 13:

Lin does not explicitly discloses A method as claimed in claim 1, wherein the second simulation is implemented using a C model.

Kim, however, discloses A method as claimed in claim 1, wherein the second simulation is implemented using a C model. **(Introduction, Paragraph 2)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize C code for the simulation as discussed in **Kim** for the simulation in **Lin** since C is commonly used higher level programming language as disclosed numerous times in **Kim**.

Regarding Claim 27:

Lin does not explicitly discloses A method as claimed in claim 15, wherein the second simulation is implemented using a C model.

Kim, however, discloses A method as claimed in claim 1, wherein the second simulation is implemented using a C model. **(Introduction, Paragraph 2)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize C code for the simulation as discussed in **Kim** for the simulation in **Lin** since C is commonly used higher level programming language as disclosed numerous times in **Kim**.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. All Claims are rejected.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

October 18, 2006

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